PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10073328	02/13/2002	~~327~~ 716	12	~~2815~~ 2825	Gavbowski

**APPLICANTS: Hasegawa Takao;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-215793 07/16/2001

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☑ yes ☐ no	ATTORNEY DOCKET NO	
35 USC 119 conditions met	☑ yes ☐ no	401558	
Verified and Acknowledged Examiners's intials			

TITLE : Method of wiring semiconductor integrated circuit, semiconductor integrated circuit, and computer product

U.S.DEPT OF COMM /PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
	Assistant Examiner	Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due / Date Paid	Primary Examiner	Sheets Drwg. / Figs.Drwg.	Print Fig.
☐ TERMINAL DISCLAIMER	PREPARED FOR ISSUE	Application Examiner	

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